PCI Express® Architecture PHY Test Specification Revision 2.0

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1. Introduction

This document provides test descriptions for PCI Express electrical testing. It is relevant for anyone building add-in cards or system boards to the *PCI Express Card Electromechanical Specification, Revision 2.0*. This specification does not describe the full set of PCI Express tests and assertions for these devices.

In particular, devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

PCI Express Architecture Configuration Space Test Specification

Platform BIOS Test Considerations for the PCI Express Architecture

PCI Express Architecture Link Layer Test Specification

PCI Express Architecture Transaction Layer Test Specification

1.1. Coverage

This document covers items in the *PCI Express Card Electromechanical Specification, Revision 2.0* or the *PCI Express Base Specification, Revision 2.0* that apply to 5.0 GT/s signaling and 2.5 GT/s signaling. 2.5 GT/s signaling requirements described in the *PHY Electrical Test Considerations, Revision 1.1* document apply to PCIe 1.1 and PCIe 1.0a devices that support 2.5 GT/s signaling.

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2. Test Assertions

Note: Test Assertions with Test Descriptions labeled as N/A are currently not planned for testing in the PCI Express test suite. However, the assertions must still be met.

Note: There are published PCI Express 1.1 checklists. The 1.1 assertions listed here are the assertions from the checklists documents tested by configuration test descriptions. The checklists were not updated for PCI Express 2.0.

Assertion #	Assertion Description	Test #
Subsection Reference: CEM 2.0 Specification		
CEM.1.0#1	If an add-in card or motherboard supports 5.0 GT/s it must also support 2.5 GT/s.	N/A
CEM.4.6.8#1	The PCB differential trace impedance for 5.0 GT/s capable add-in cards and motherboards must be between 68 and 105 ohms.	3.6, 3.7
CEM.4.6.9#1	The propagation delay for an add-in card from the edge finger to the Receiver/Transmitter must not exceed 750 ps.	3.6
CEM.47.2#1	The add-in card eye opening at 5.0 GT/s and 3.5 dB must not be less than 380 mV.	3.1
CEM.4.7.2#2	The add-in card differential signaling at 5.0 GT/s and 3.5 dB must not exceed .6 V or be less than - .6 V.	3.1
CEM.4.7.2#3	The add-in card total jitter with compliance pattern at 5.0 GT/s and 3.5 dB at a BER of 10^{-12} must not exceed 77 ps.	3.1
CEM.4.7.2#4	The add-in card differential eye opening at 5.0 GT/s and 6.0 dB must not be less than 306 mV on non-deemphasized bits.	3.1
CEM.4.7.2#4	The add-in card differential eye opening at 5.0 GT/s and 6.0 dB must not be less than 260 mV on deemphasized bits.	3.1
CEM.4.7.2#6	The add-in card differential signaling at 5.0 GT/s and 6.0 dB must not exceed .6 V or be less than - .6 V.	3.1

Assertion #	Assertion Description	Test #
CEM.4.7.2#7	The add-in card total jitter with compliance pattern at 5.0 GT/s and 6.0 dB at a BER of 10^{-12} must not exceed 77 ps.	3.1
CEM.4.7.2#8	The add-in card deterministic jitter with compliance pattern at 5.0 GT/s and 3.5 dB must not exceed 57 ps.	3.1
CEM.4.7.2#9	The add-in card deterministic jitter with compliance pattern at 5.0 GT/s and 6.0 dB must not exceed 57 ps.	3.1
CEM.4.7.6#1	The motherboard differential eye opening at 5.0 GT/s and the de-emphasis level(s) that will be used in normal operation must not be less than 300 mV	3.2
CEM.4.7.6#2	The motherboard differential signaling at 5.0 GT/s and the de-emphasis level(s) that will be used in normal operation must not exceed .6 V or be less than -.6 V.	3.2
CEM.4.7.6#3	The motherboard 2 port total jitter at a BER of 10^{-12} with compliance pattern at 5.0 GT/s with the de-emphasis level(s) that will be used in normal operation must be less than 105 ps.	3.2
CEM.4.7.6#4	The motherboard 2 port deterministic jitter with compliance pattern at 5.0 GT/s with the de-emphasis level(s) that will be used in normal operation must be less than 57 ps.	3.2
Subsection Reference: Base 2.0 Specification		
BASE.4.3.3.1#1	The add-in card PLL bandwidth when measured with compliance pattern must be between 5 and 16 MHz if the peaking is less than 1 dB or must be between 8 and 16 MHz with a peaking of less than 3 dB.	3.5
BASE.4.2.6.2.2#1	The add-in card or motherboard is required to switch compliance modes in the following order each time a 1 ms, 100 MHz, differential signal with at least 350 mV peak to peak amplitude is applied to receive lane zero: 2.5 GT/s and 3.5 dB, 5.0 GT/s and 3.5 dB, 5.0 GT/s and 6.0 dB.	3.1 3.2

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3. Test Descriptions

3.1. Add-in Card Signal Quality

This test is run on all card electromechanical form factor add-in cards. The test verifies that the signaling of the add-in card at 5.0 GT/s with 3.5 dB of de-emphasis and 5.0 GT/s with 6.0 dB of de-emphasis and 2.5 GT/s with 3.5 dB of de-emphasis meets eye diagram and other jitter requirements.

Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

Overview of Test Steps

The test performs the following steps.

1. Insert the add-in card under test into a compliance base board (CBB) revision 2.0 without power.
2. Terminate all lanes except the lane under test.
3. Connect the lane under test to a high speed oscilloscope via SMP to SMA adaptors and phase matched SMA cables or phase matched SMP to SMA cables.
4. Power on the CBB.
5. Measure transmitted waveform with high speed oscilloscope.
6. Confirm that waveform is compliance pattern.
7. Inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test. (Push compliance toggle button on CBB.)
8. Repeat steps 5-7 until compliance pattern is observed at 2.5 GT/s and then one additional time. Verify that compliance mode is at 5.0 GT/s (or continue through step 15 if the DUT is a PCIe 2.0 2.5 GT/s only capable device).
9. Capture at least 1 million UI * 200 ps of data at a sample rate of no more than 25 ps (or 250,000 UI * 400 ps of data at a sample rate of no more than 50 ps for 2.5 GT/s)
10. Compute the eye diagram and compare with PCI Express Card Electromechanical Specification requirements for 5.0 GT/s signaling with 3.5 dB de-emphasis.

11. Compute random, deterministic, and total jitter at a 10^{-12} BER using the dual dirac method and compare with the PCI Express Card Electromechanical Specification requirements for 5.0 GT/s signaling with 3.5 dB de-emphasis.
12. Compute the average data rate and verify that it is within 5.0 Gb/s +/- .03%.
13. Inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test. (Push compliance toggle button on CBB.)
14. Repeat steps 9-11 comparing against the PCI Express card electromechanical requirements with 6.0 dB de-emphasis.
15. Repeat steps 2-14 for all lanes.
16. Repeat steps 2-15, except comparing against the PCI Express card electromechanical requirements at 2.5 GT/s signaling and 3.5 dB de-emphasis (if the DUT is a 5 GT/s capable device).

The test *fails* if:

- Compliance mode is not supported correctly.
- Eye diagram or extrapolated/RJ jitter limit requirements are not met at any of the required compliance mode states.

3.2. System Board Signal Quality

This test is run on all card electromechanical form factor system boards. The test verifies that the signaling of the system at 5.0 GT/s with 3.5 dB of de-emphasis, 5.0 GT/s with 6.0 dB of de-emphasis, and 2.5 GT/s with 3.5 dB of de-emphasis meets eye diagram and other jitter requirements.

Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

Overview of Test Steps

The test performs the following steps.

1. Power down the system under test.
2. Insert the compliance load board (CLB) revision 2.0 into the slot for test.
3. Terminate all lanes except the lane under test.
4. Connect the lane under test to a high speed oscilloscope via SMP to SMA adaptors and phase matched SMA cables or phase matched SMP to SMA cables.
5. Power on the system under test.
6. Connect the clock signal to the oscilloscope under test via reference clock SMP connectors on the CLB. The clock must have SSC enabled or disabled to be consistent with settings for the system during normal operation.

7. Measure transmitted clock and data waveforms simultaneously with high speed oscilloscope.
8. Confirm that the data waveform is compliance pattern.
9. Inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the system board under test. (Push compliance toggle button on CBB.)
10. Repeat steps 7-9 until compliance pattern is observed at 2.5 GT/s and then one additional time if the lane under test will operate at 3.5 dB de-emphasis in normal operation and two additional times if the lane under test will operate at 6.0 dB de-emphasis during normal operation. Verify that compliance mode is at 5.0 GT/s.
11. Capture at least 1 million * 200 ps of data and clock simultaneously at a sample rate of no more than 25 ps (or 250,000 UI * 400 ps of data at a sample rate of no more than 50 ps for 2.5 GT/s).
12. Compute eye diagram and compare with PCI Express system board electromechanical specification requirements for 5.0 GT/s.
13. Compute random, deterministic, and total jitter at a 10^{-12} BER using the dual dirac method and compare with PCI Express card electromechanical specification requirements for system board signaling at 5.0 GT/s.
14. Compute the average data rate for the DATA and verify that it is within 5.0 Gb/s +/- .03% if SSC is not present and 5.0 GB/s +.03/-.53% if SSC is present.
15. Repeat with each lane as the lane under test.
16. Repeat for all 5.0 GT/s capable slots on the system under test.
17. Repeat steps 1-16 for all PCIe 2.0 2.5 GT/s only capable slots and 5.0 GT/s capable slots on the system under test, except operating the slots at 2.5 GT/s and 3.5 dB of de-emphasis.

The test *fails* if:

- Compliance mode is not supported correctly.
- Eye diagram or extrapolated/RJ jitter limit requirements are not met at any of the required compliance mode states.

3.3. Add-in Card Receive Packet Error Rate

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card can function normally in system(s) with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Overview of Test Steps

The test performs the following steps.

1. Insert the add-in card under test into a system selected for test. (Selected systems must be PCIe 2.0 5.0 GT/s capable or PCIe 2.0 2.5 GT/s capable and pass system signal quality requirements.)
2. Power on system normally.
3. Verify that link forms at 5.0 GT/s and add-in card can successfully demonstrate normal operation (provide normal functionality to a user).

4. Retrain with system configured to initialize loopback mode using modified compliance pattern at 5.0 GT with the de-emphasis level used by the system link during normal operation.
5. Run loopback pattern for 20 minutes.
6. Check the error count reported by the add-in card under test with the modified compliance pattern (and the receive error count for the system if possible).
7. Verify that neither error rate exceeds a BER target of 10^{-12}.
8. Repeat steps 1- 7, except run the test at 2.5 GT/s and 3.5 dB of de-emphasis.
9. Repeat testing for all selected systems.

The test *fails* if:
The BER rate exceeds E-12.

3.4. System Receive Packet Error Rate

This test is run on all card electromechanical form factor systems. The test verifies that the system can function normally with add-in card(s) with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Starting Configuration

Overview of Test Steps

The test performs the following steps.

1. Insert a selected add-in card under test into the system under test. (Selected add-in cards must be PCIe 2.0 5.0 GT/s or PCIe 2.0 2.5 GT/s capable and pass system signal quality requirements.)
2. Power on system normally.
3. Verify that link forms at 5.0 GT/s and add-in card can successfully demonstrate normal operation (provide normal functionality to a user).
4. Retrain with system configured to initialize loopback mode using modified compliance pattern at 5.0 GT with the de-emphasis level used by the system link during normal operation.
5. Run loopback pattern for 20 minutes.
6. Check the error count reported by the system under test with the modified compliance pattern (and the receive error count for the system if possible).
7. Verify that neither error rate exceeds a BER target of 10^{-12}.
8. Repeat steps 1-7, except run the test at 2.5 GT/s.
9. Repeat testing for all selected add-in cards.

The test *fails* if:
The BER rate exceeds E-12.

3.5. Add-in Card PLL Bandwidth

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card PLL bandwidth and peaking are within the limits allowed by the PCI Express specifications.

Starting Configuration

Overview of Test Steps

The test performs the following steps.

1. Insert a selected add-in card under test into a CBB without power.
2. Connect one of the following two options to provide a reference clock with modulation for the PLL bandwidth test:
 a. Connect a signal generator to the noise injection port on the CBB. Note that the CBB may need to be modified to enable the port.

 The signal generator must be able to provide a signal that induces phase jitter on the reference clock from 0 to 25 MHz.

 Note: Approach 2a will work with PLL designs that use only the rising edge of the reference clock.

 b. Connect an external source to the CBB reference clock input.
 The external source must be able to provide a 100 MHz reference clock signal with phase jitter from 0 to 25 MHz.

 Note: Approach 2b will work with PLL designs that use only the rising edge of the reference clock or both edges of the reference clock.
3. Connect the output of transmit lane zero to an instrument capable of measuring the transmitter frequency response as a function of the frequency of phase jitter on the reference clock.
4. Power on the CBB normally.
5. Measure transmitter output.
6. Confirm that the transmitter output is compliance pattern.
7. Inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test. (Push compliance toggle button on CBB.)
8. Repeat steps 5-7 until compliance pattern is observed at 2.5 GT/s and then one additional time. Verify that compliance mode is at 5.0 GT/s.
9. Apply modulation on the reference clock producing phase jitter from 0 to 25 MHz. The modulated reference clock is calibrated such that the measured reference clock phase jitter is within 20% of the limit allowed for a reference clock by the PCI Express 2.0 Specification.. Measure the transmitter output on lane zero across this range.
10. Analyze the transmitter output and estimate the reference clock phase jitter frequency where the transmitter response is -3 dB. Also note the maximum amplitude of the transmitter output.
11. The -3 dB point must fall between 5 and 16 MHz if the maximum peaking is less than 1 dB and between 8 and 16 MHz if the transmitter peaking is less than 3 dB. The maximum peaking must not exceed 3 dB.

12. Repeat steps 9-11 with the amplitude set to ½ of the initial calibrated noise amplitude value.
13. Repeat the test at 2.5 GT/s. The 3 dB point must fall between 1.5 and 22 MHz with peaking less than 3 dB.

3.6. Add-in Card PCB Impedance

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card TX and RX path PCB differential trace impedance is in the range required by the PCI Express 2.0 Card Electromechanical Specification.

1. Connect TDR to TX lane zero of a CBB without an add-in card and without power.
2. Measure impedance with the TDR rise time set to 50 ps. Note the time to the open circuit discontinuity – this time will be referenced as the edge-finger reference location.
3. Insert a selected add-in card under test into a CBB without power. The test is conducted with power off.
4. Measure the impedance with the TDR. The impedance must be between 65 and 105 ohms from the edge finger reference locations to the terminations.

 Note that exceptions are allowed as specified in the PCI Express Card Electromechanical Specification, Revision 2.0.
5. Verify that the time from the edge-finger reference location to the terminations does not exceed 750 ps.
6. Repeat steps 1-5 for all other TX lanes.
7. Repeat steps 1-5 for all RX lanes.

3.7. System Board PCB Impedance

This test is run on all card electromechanical form factor systems. The test verifies that the system board TX and RX path PCB differential trace impedance is in the range required by the PCI Express 2.0 Card Electromechanical Specification.

1. Connect TDR to TX lane zero of a CLB that is not connected to a motherboard.
2. Measure impedance with the TDR rise time set to 50 ps. Note the time to the open circuit discontinuity – this time will be referenced as the connector reference location.
3. Insert the CLB into the slot of the motherboard under test. The test is conducted with the motherboard power off.
4. Measure the impedance with the TDR. The impedance must be between 65 and 105 ohms from the connector reference locations to the terminations.

 Note that exceptions are allowed as specified in the PCI Express Card Electromechanical Specification, Revision 2.0.
5. Repeat steps 1-4 for all other TX lanes.
6. Repeat steps 1-4 for all RX lanes.

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